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EXAMINER	
BLAIR, KILE O	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,342	MAGRATH, ANTHONY J.	
	Examiner	Art Unit	
	Kile O. Blair	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-27,29,30 and 32-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-27,29,30 and 32-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to the communication filed on 6/11/2008. Claims 1-9, 11-27, 29-30, and 32-39 are pending.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 32 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claim 32 recites processor control code that is not embodied in a computer readable medium or other machine capable of carrying out the instructions of the control code. Since processor control code (i.e. a computer program) is merely a set of instructions capable of being executed by a computer, the computer program itself is not a process and a claim for a computer program, without the computer-readable medium needed to realize the computer program's functionality, is nonstatutory functional descriptive material. See MPEP § 2106.01

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 13-24, 29, 30, 34-36 and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 13 recites the limitation "said signal". There is insufficient antecedent basis for this limitation in the claim. Although claim 13 previously recites "a digital audio signal", claim 1 which is incorporated into claim 13 recites a gain signal and a volume control signal. Claim 13 relies on claim 1 for antecedent basis for the recitation of "said gain signal"; therefore the examiner looks to the prior portion of claim 13 as well as claim 1 for antecedent basis for the recitation of "said signal." It is unclear which previously recited signal (i.e. digital audio signal, volume control signal, or gain signal) is referred to, although it appears that the applicant intends to recite "said digital audio signal." Claim 17 is rejected for the recitation of "said signal" for the same reasons as claim 13. The examiner recommends that claims 13 and 17 be amended to recite "said digital audio signal."

Claims 14-24, 29, 30, 34-36, and 39 are further rejected for incorporating the above errors of the claims on which they depend or otherwise incorporate.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2-6, 13-20, 22-27, 29, 30, 32-37, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thomas (US Pat. No. 4,947,133).

Regarding claim 1, as it provides basis for claims 2-5, Thomas teaches a gain determining stage for determining a gain signal to be applied to amplify an audio signal, the stage comprising:

an input for receiving a parameter (the input of adder 28 that receives $Log(V_{pk})$ signal, fig. 3, col. 6, lines 19-21) of said audio signal (input signal at V_I, fig. 3);

an adjuster for adjusting said parameter (adder 28 adjusts $Log(V_{pk})$ by adding $Log(G_A)$, fig. 3) dependent on a received volume control signal (summed output of adder 28 depends on volume control signal $Log(G_A)$, fig. 3); and

a gain selector for applying a variable gain function (adder 27 for applying a variable function: $G_{(gain)}=2^{LogG}$, where $LogG=Log(G_A)+Log(G_W)$; fig. 3) to said volume control signal ($Log(G_A)$, fig. 3) in order to generate a gain signal for applying to the audio signal (signal $Log(G_A)+Log(G_W)$ at output of adder 27, fig. 3)

wherein said gain function is dependent on said adjusted parameter (the gain function $\{logG=Log(G_A)+Log(G_W)\}$ is dependent on $Log(V_{pk})+Log(G_A)$, i.e. the adjusted parameter, because the gain function incorporates, and is therefore dependent on, $Log(G_W)$ and $Log(G_W)$ is derived from, and is therefore dependent on (see compression function 23, fig. 3), the adjusted parameter: $Log(V_{pk})+Log(G_A)$.

Although Thomas does not explicitly teach the feature wherein the inputted audio signal V_I is a digital signal, Thomas does teach that the signal path will be analog and

the control path is digital as shown in figure 4. It would have been obvious to one of ordinary skill in the art to implement the speech controller of figure 3 of Thomas as a completely digital circuit by moving the ADC 30 of figure 4 in front of the input signal V_I, replacing the delay 10 formed by a CCD (col. 6, lines 30-33) with a digital delay, and replacing the gain controlled amplifier 11 formed by an MDAC (col. 6, lines 30-33) with a digital multiplier followed by a DAC. Such a modification of the teachings of Thomas is the substitution of known equivalents for the same purpose (i.e. replacing known analog circuit elements with known digital elements to yield predictable results) and therefore would have been obvious to one of ordinary skill in the art. See MPEP § 2144.06, II.

Regarding claim 2, Thomas teaches a gain determining stage according to claim 1 wherein the received volume control signal is input to a processor before being passed to the adjuster (the gain function G_A is inherently sent to a log converter before being passed to adder 28 as $\text{Log}(G_A)$, i.e. the adjuster, fig. 3).

Regarding claim 3, Thomas teaches a gain determining stage according to claim 2 wherein the processor comprises a log converter and/or a scaling means (inherent log converter, see rejection to claim 2).

Regarding claim 4, Thomas teaches a gain determining stage according to claim 1 wherein the adjuster comprises an adder for adding the volume control signal to the log converted parameter (adder 28, fig. 3).

Although Thomas does not explicitly teach the feature wherein the adjuster comprises a log converter for log converting the received parameter, it would have been

obvious to one of ordinary skill in the art to move the log converter 26 (fig. 3) into the adder 28 (i.e. adjuster) as a simple rearrangement of parts with predictable results.

Regarding claim 1, as it provides basis for claims 1, 5, 6, 13-24, 29, 30, 34-36, and 39, Thomas teaches a gain determining stage for determining a gain signal to be applied to amplify an audio signal, the stage comprising:

an input for receiving a parameter (the input of adder 28 that receives $Log(G_A)$ signal, fig. 3, col. 6, lines 19-21) of said audio signal (input signal at V_i, fig. 3);

an adjuster for adjusting said parameter (compression function 23 and adder 28 adjust $Log(G_A)$ to produce $Log(G_W)$, i.e. the adjusted parameter, fig. 3) dependent on a received volume control signal (output of compression function 23 is dependent on select waveshape compression signal, fig. 3); and

a gain selector for applying a variable gain function (adder 27 for applying a variable gain function: $G_{(gain)}=2^{LogG}$, where $LogG=Log(G_A)+Log(G_W)$; fig. 3) to said volume control signal (select waveshape compression signal is incorporated in G_W, therefore the variable gain function is applied to the select waveshape compression signal since it is applied to G_W), fig. 3) in order to generate a gain signal for applying to the audio signal (signal $Log(G_A)+Log(G_W)$ at output of adder 27, fig. 3)

wherein said gain function is dependent on said adjusted parameter (the gain function {$logG=Log(G_A)+Log(G_W)$} is dependent on $Log(G_W)$).

Although Thomas does not explicitly teach the feature wherein the inputted audio signal V_i is a digital signal, Thomas does teach that the signal path will be analog and

the control path is digital as shown in figure 4. It would have been obvious to one of ordinary skill in the art to implement the speech controller of figure 3 of Thomas as a completely digital circuit by moving the ADC 30 of figure 4 in front of the input signal V_I, replacing the delay 10 formed by a CCD (col. 6, lines 30-33) with a digital delay, and replacing the gain controlled amplifier 11 formed by an MDAC (col. 6, lines 30-33) with a digital multiplier followed by a DAC. Such a modification of the teachings of Thomas is the substitution of known equivalents for the same purpose (i.e. replacing known analog circuit elements with known digital elements to yield predictable results) and therefore would have been obvious to one of ordinary skill in the art. See MPEP § 2144.06, II.

Regarding claim 5, Thomas teaches a gain determining stage according to claim 1, as it provides basis for claims 1, 5, 6, 13-24, 29, 30, 34-36, and 39, wherein the parameter is dependent on the peak value of the received signal ($Log(V_{pk})$ is the output of the peak detector, col. 3, lines 5-7, fig. 3).

Regarding claim 6, Thomas teaches a gain determining stage according to claim 5 wherein the parameter is a peak level envelope signal (the smoothing means 14 and the gain function 15 derive an envelope control signal from peaks out of the queue, col. 4, lines 37-40, fig. 3).

Regarding claim 13, Thomas teaches a signal processing circuit for amplifying a digital audio signal, comprising:

a parameter determining processor for determining a parameter of said signal (peak detector 12, smoothing function 14, and gain function 15, fig. 3);

a gain determining stage according to claim 1 (see rejection of claim 1 as it provides

basis for claims 1, 5, 6, 13-24, 29, 30, 34-36, and 39); and

an amplifier for amplifying said signal according to said gain signal (gain controlled amplifier A1, fig. 3).

Regarding claim 14, Thomas teaches a circuit according to claim 13 wherein the parameter determining processor is a peak detector (peak detector 12, smoothing function 14, and gain function 15, fig. 3).

Regarding claim 15, Thomas teaches a circuit according to claim 14 wherein the peak detector output is dependent on the peak levels in the signal waveform (fig. 3) and a time dependent decay characteristic (time constant R_2C with a long time constant for decaying, i.e. downward trends, col. 3, lines 37-45) wherein the decay characteristic is further dependent on the frequency of said signal (the smoothing means 14 has a sampling period equal to the arrival time of each new peak value and hence the filter time constant adapts to frequency of the input, col. 5, lines 38-46).

Regarding claim 16, Thomas teaches a circuit according to claim 15 wherein the peak detector comprises a disabler for disabling the decay characteristic until the signal changes polarity (the smoothing detector means 14 only creates a new smoothed output at each zero crossing, col. 3, lines 21-24).

Regarding claim 17, Thomas teaches a circuit according to claim 13 further comprising a delay for delaying said signal prior to said amplification in order to first determine said gain characteristic (delay 10, fig. 3).

Regarding claim 18, Thomas teaches a circuit according to claim 14 comprising: an input for receiving a signal (input V_I, fig. 3); a peak level processor for determining

peak levels in the signal (peak detector 12, fig. 3); and an output for outputting a signal dependent on said peak levels (output V_O, fig. 3) and a time dependent decay characteristic (time constant R_2C with a long time constant for decaying, i.e. downward trends, col. 3, lines 37-45), wherein the decay characteristic is further dependent on the frequency of said received signal (the smoothing means 14 has a sampling period equal to the arrival time of each new peak value and hence the filter time constant adapts to frequency of the input, col. 5, lines 38-46).

Regarding claim 19, Thomas teaches a detector according to claim 18 wherein the output comprises a disabler for disabling the decay characteristic until the signal changes polarity (the smoothing detector means 14 only creates a new smoothed output at each zero crossing, col. 3, lines 21-24).

Regarding claim 20, Thomas teaches a circuit according to claim 14 comprising:

an input to receive an input audio signal (input V_I, fig. 3);

an amplitude processor operable in a decay mode (smoothing means 14 with time constant R_2C with a long time constant for decaying, i.e. downward trends, col. 3, lines 37-45),

being when the input audio signal is smaller than a previous output signal (downward trends, col. 3, lines 37-45), whereby in the decay mode, the processor is configured to generate a signal for decreasing the amplitude of a signal to be output (downward trends, col. 3, lines 37-45); and

a logic device for controlling the operation of the amplitude processor in the decay mode such that the processor only generates a signal in the decay mode upon

receipt of a trigger from the logic device (the smoothing detector means 14 only creates a new smoothed output at each zero crossing, col. 3, lines 21-24, as determined by zero crossing director 16, i.e. a logic device),

whereby the trigger is related to the frequency of the input audio signal (zero crossings occur according to the frequency of the signal).

Claim 21 is substantially similar to claim 20 and is rejected for the same reasons.

Regarding claim 22, Thomas teaches the signal level detector of claim 20 further comprising a comparator for determining when a change of sign occurs (zero crossing detector compares output of delay to output of queue, col. 6, lines 43-44), wherein the comparator is associated with the logic device (the zero crossing detector is interpreted to be a comparator and a logic device), and the logic device sends a trigger to the amplitude processor when a change of sign of the input signal occurs (the smoothing detector means 14 only creates a new smoothed output at each zero crossing, col. 3, lines 21-24, as determined by zero crossing director 16, i.e. a logic device).

Regarding claims 23 and 24, Thomas teaches the signal level detector of claim 20.

Although Thomas does not explicitly teach the feature wherein the logic device comprises an input for receiving a timeout signal, and the logic device sends a trigger to the processor when a timeout signal is received and further comprising a timeout counter which is configured to generate the timeout signal after a time period passes, corresponding to the lowest frequency of the input signal, without a change of sign occurring, Thomas does teach a high pass filter to limit the maximum interval between

zero crossings to not exceed the signal path delay of 10ms which corresponds to the lowest frequency of 100Hz (col. 6, line 58- col. 7, line 1). Therefore it would have been obvious to one of ordinary skill in the art to implement a timeout as an alternative to pre-filtering with the motivation of limiting the maximum interval between zero crossings as disclosed by Thomas (col. 6, line 58- col. 7, line 1).

Regarding claim 25, Thomas teaches a method according to claim 38 wherein determining the peak level envelope comprises:

receiving an input audio signal (input signal at V_I, fig. 3);

comparing the input audio signal with a previous output signal to obtain a difference signal (determining upward and downward trends, col. 3, lines 40-45);

generating a scaled signal by scaling the difference signal using an attack coefficient or a decay coefficient, depending upon the comparison (two separate time constants based on upward and downward trends, col. 3, lines 37-45);

combining the scaled signal with the previous output signal to obtain a signal, indicative of the signal level of the input audio signal (weighted sum of successive peaks, col. 3, lines 46-52), characterized in that the method comprises:

controlling the generation of the scaled signal when scaled by the decay parameter (time constant R_2C with a long time constant for decaying, i.e. downward trends, col. 3, lines 37-45), using a trigger related to the frequency of the input audio signal (the smoothing means 14 has a sampling period equal to the arrival time of each new peak value and hence the filter time constant adapts to frequency of the input, col. 5, lines 38-46).

Claim 26 is substantially similar to claim 15 and is rejected for the same reasons.

Claim 27 is substantially similar to claim 16 and is rejected for the same reasons.

Regarding claim 29, Thomas teaches an integrated circuit comprising a circuit according to claim 13 (col. 7, lines 10-12).

Regarding claim 30, Thomas teaches audio equipment comprising an integrated circuit according to claim 29 (col. 7, lines 10-12).

Regarding claim 32, Thomas teaches processor control code configured to implement the signal processing method of claim 37 (col. 7, lines13-26, fig. 5).

Regarding claim 33, Thomas teaches a computer-readable medium comprising the processor control code of claim 32 (col. 7, lines 13-26, fig. 5).

Claim 34 is substantially similar to claim 22 and is rejected for the same reasons.

Claim 35 is substantially similar to claim 23 and is rejected for the same reasons.

Claim 36 is substantially similar to claim 24 and is rejected for the same reasons.

Claim 37 is substantially similar to claim 1, as it provides basis for claims 1, 5, 6, 13-24, 29, 30, 34-36, and 39, and is rejected for the same reasons.

Claim 38 is substantially similar to claim 6 and is rejected for the same reasons.

Regarding claim 39, Thomas teaches a method of amplifying a digital audio signal, comprising:

determining a parameter of said signal (peak detector 12, smoothing function 14, and gain function 15, fig. 3);

determining a gain signal according to claim 24 (see rejection of claim 24); and

amplifying said digital audio signal by applying said gain signal (gain controlled amplifier A1, fig. 3).

Claims 1 and 7-9, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Engebretsen (US Pat. No. 5,724,433).

Regarding claim 1, Engebretson teaches a gain determining stage for determining a gain signal to be applied to amplify a digital audio signal (input converted into digital by D/A converter, col. 4, lines 28-30), the stage comprising: an input for receiving a parameter of said digital audio signal (input 12 receives amplitude of signal, fig. 2); an adjuster (amplifier 78, col. 7, lines 22-25, fig. 2) for adjusting said parameter dependent on a received volume control signal (signal on line 76, col. 7, lines 20-22, fig. 2); and a gain selector for applying a variable gain function to said volume control signal in order to generate a gain signal for applying to the digital audio signal (gain control 66, col. 7, lines 14-16, fig. 2).

Although Engebretson does not explicitly teach the feature wherein said gain function is dependent on said adjusted parameter, it would have been obvious to one of ordinary skill in the art to use the same volume control signal on lines 18 and 76 in figure 2 with the motivation of simplifying the circuit and eliminating components such as registers 22 and 74.

Regarding claim 7, Engebretson teaches a gain determining stage according to claim 1 further comprising: an input to receive a threshold signal (line from threshold register to comparator, col. 4, lines 50-52, fig. 2); and a comparator for comparing an

output of the adjuster with the threshold signal (comparator 32, col. 4, lines 50-52, fig. 2), wherein the gain selector determines the gain dependent on the comparison (the gain control 66 depends on the signal from line 68 which is dependent on comparator output 36, fig. 2).

Regarding claim 8, Engebretson teaches a gain determining stage according to claim 7 wherein the threshold signal is input to a processor before being passed to the comparator (the circuits of figures 1-9 use log encoded data, col. 9, lines 47-49).

Regarding claim 9, Engebretson teaches a gain determining stage according to claim 8 wherein the processor comprises a log converter and/or a scaling means (the circuits of figures 1-9 use log encoded data, col. 9, lines 47-49).

Regarding claim 11, Engebretson teaches the gain determining stage of claim 7 wherein the gain is determined using a variable gain function as follows: when the output of the adjuster is greater than the threshold signal (when the level of the output signal of amplifier 16 exceeds the threshold level stored in register 34, comparator 32 outputs a high signal via line 36, col. 4, lines 52-55), a negative signal polarity is utilized (when multiplexer 38 receives a high signal via line 36, multiplexer 38 outputs a negative value corresponding to dm via a line 44, col. 4, lines 60-62); or when the output of the adjuster is less than the threshold signal (when the level of the output of amplifier 16 falls below the threshold level stored in register 34, comparator 32 outputs a low signal via line 36, col. 4, lines 55-57), a positive signal polarity is utilized (when multiplexer 38 receives a low signal via line 36, multiplexer 38 outputs a positive value corresponding to dp via line 44, col. 4, lines 62-64).

Regarding claim 12, Engebretson teaches the gain determining stage of claim 11.

Although Engebretson does not explicitly teach the feature wherein the variable gain function, or a factor of the variable gain, is: $K = 2^{lgK}$ where $lgK = lgGs + m(lgGV + lgTA)$ where K is the gain, $lgGs$ is the volume control signal, $lgGV$ is the output of the adjuster, $lgTA$ is the threshold signal and m is a value indicative of a predetermined operational characteristic curve, Engebretson teaches a variable gain function based on a compression ratio as shown in figure 3 and it would have been obvious to one of ordinary skill in the art to implement the gain determining stage of Engebretson in accordance with the recited equation as a matter of designer's preference.

Response to Arguments

Applicant's arguments with respect to claims 1-9, 11-27, 29-30, and 32-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kile O. Blair whose telephone number is (571) 270-3544. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on (571) 272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KB

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